REMARKS

Claims 1-2, 6-9, and 12-14 are amended, no claims are canceled, and no claims are added; as a result, claims 1-16 are now pending in this application.

No new matter has been added through the amendments to claims 1-2, 6-9, and 12-14. Support for the amendments to claims 1-2, 6-9, and 12-14 may be found throughout the specification, for example but not limited to, the specification at page 7, line 22 through page 11, line 2, and in FIG. 2 as originally filed in the application.

§102 Rejection of the Claims

Claims 6-16 were rejected under 35 U.S.C. § 102(b) as being anticipated by Kennedy (U.S. 5,659,748). Applicant respectfully traverses the rejection of claims 6-16.

Claims 6-16 are not anticipated by Kennedy because Kennedy fails to disclose the claimed subject matter included in claims 6-16. By way of example, but not limited to this example, independent claim 6 as now amended includes,

> a first processor designated as a bootstrap processor;
> a latch including a set input and a reset input, and including an output coupled to said bootstrap processor for turning off said bootstrap processor;
> a control unit including a timer coupled to the set input for providing a first control signal for setting said latch, the control unit including a second control signal coupled to the reset input for resetting said latch, and at least one additional control signal for controlling additional processors;
> a watchdog timer coupled to the set input for setting said latch, wherein the control unit includes a third control signal coupled to a reset input of the watchdog timer for resetting the watchdog timer.

Thus, claim 6 includes a latch including a set input, a control unit including a timer coupled to the set input of the latch, and a watchdog timer couple to the set input of the latch. In contrast, Kennedy concerns slot select circuits wherein,[1]

> FIG. 4 illustrates the logic 148 corresponding to the slot select circuits 148A and 148B and slot select circuits for any other

[1] *See* Kennedy at column 6, lines 33-52.

> CPU installed in the system. The slot select logic 148 comprises AND gates 172, 174, 176, a NAND gate 178, an EXOR gate 180, OR gates 182, 183, a timer 184, time select logic 185, a latch 186, and inverters 188, 189, 190, 191, and 192. The timing circuit responds to signals on a SLOT_ SELECT signal line 193, SLOT_ ID (SID0, SID1, SID2, SID3) signal lines 194-197, a CLOCK signal line 200, a CLK signal line 202, a BD_ RESET- signal line 204, and a CPU_ RESET- signal line 206. The slot select circuit 148 provides a signal on a RESET- signal line 208 connected to the reset pin of the microprocessor 209 on the CPU board. The slot select circuit 148 further responds to a number of internal signal lines, such as a SLOT_ ONE signal line 210, a SLOT_ ONE- signal line 212, a SLOT_ SELECT- signal line 214, a TERM- signal line 216, a RUN- signal line 218, a SLOT_ 1_ RESET- signal line 220, a RUN signal line 221, and a STOP- signal line 222.

Thus, Kenney describes logic including a timing circuit and a latch, but fails to disclose for example, "a latch including a set input and a reset input, and including an output coupled to said bootstrap processor for turning off said bootstrap processor; . . . a control unit including a timer coupled to the set input for providing a first control signal for setting said latch, . . . a watchdog timer coupled to the set input for setting said latch, . . ." as required by independent claim 6.

Because Kennedy fails to disclose all of the subject matter included in independent claim 6, independent claim 6 is not anticipated by Kennedy.

In another example of claimed subject matter not disclosed by Kennedy, independent claim 12 includes,

> a control unit including a timer, the control unit operable for generating a plurality of control signals;
>
> a watchdog timer including a watchdog timer reset input coupled to a fourth of the plurality of control signals;
>
> a latch including a set input, a reset input and a latch output, the set input coupled to an output of the watchdog timer and to a first of the plurality of control signals, the reset input coupled to a second of the plurality of control signals, and the latch output coupled to said bootstrap processor for turning said bootstrap processor off;

> said watchdog timer providing a signal indicating that a predetermined time has expired, which is applied to said latch to set said latch;
>
> said control unit providing the first control signal to said latch for setting said latch, the second control signal applied to said latch for resetting said latch, a third control signal for controlling other processors and the fourth control signal for resetting the watchdog timer.

For at least the reasons stated above with respect to independent claim 6, Kennedy fails to disclose, "a control unit including a timer, . . . a watchdog timer including a watchdog timer reset input coupled to a fourth of the plurality of control signals; . . . a latch including a set input, a reset input and a latch output, the set input coupled to an output of the watchdog timer and to a first of the plurality of control signals," as required by independent claim 12.

Because Kennedy fails to disclose all of the subject matter included in independent claim 12, independent claim 12 is not anticipated by Kennedy.

Dependent claims 7-11 depend from independent claim 6, and so include all of the subject matter included in independent claim 6, and more. Dependent claims 13-16 depend from independent claim 12, and so include all of the subject matter included in independent claim 12, and more. For at least the reasons stated above with respect to independent claim 6 and independent claim 12, Kennedy fails to disclose the subject matter included in dependent claims 7-11 and 13-16. Therefore, claims 7-11 and 13-16 are not anticipated by Kennedy.

Applicant respectfully requests reconsideration and withdrawal of the 35 U.S.C. § 102(b) rejection, and allowance of claims 6-16.

§103 Rejection of the Claims

Claims 1-5 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Natu (U.S. 5,790,850) in view of Kennedy (U.S. 5,659,748). Applicant respectfully traverses the rejection of claims 1-5.

The Office Action fails to meet the requirements for forming the proposed combination of Natu and Kennedy, and thus fails to meet the burden for establishing a prima facie case of obviousness with respect to claims 1-5.

The Office Action fails to provide proper evidence to support a suggestion or motivation to combine[2] Natu and Kennedy, as so fails to show how these documents, or any other evidence of record, suggests the desirability[3] of the proposed combination of Natu and Kennedy, thus fail to meet the burden for establishing a *prima facie* case of obviousness with respect to claims 1-5. In an attempt to meet these requirements, the Office Action states,

> It would have been obvious to one or ordinary skill in the art at the time the invention was made to modify Natu to include setting a latch for disabling bootstrap processor if the testing indicates failure, because **if the failing processor has internal failure, it may not be able to operate properly to remove itself form the operation.** Thus, disabling the failing processor eliminates the problem of relying on a failing processor to perform the appropriate action to remove itself from operation. (Emphasis added).

However, these statements appear to be contradicted by the written description of Natu, which states,[4]

> The method and apparatus of the present invention **allows a multiprocessor computer system to initialize properly even when the processor that is designated as the BSP after a hard reset of the computer system fails.** The present invention also prevents a processor that has failed previously from becoming the BSP.
>
> In the present invention, **the designated BSP determines it has failed after examining its corresponding status bits.** In the present invention, the designated BSP determines it has failed after examining its corresponding status bits. The BSP is determined to have failed if its status bits reflect that it has failed during the current boot, or any previous boot. **The designated BSP then selects a processor from among the APs that will take the place of the designated BSP.** The selection is accomplished by, successively for every AP indicated to be good by examining its corresponding status flag, determining whether the AP is present, starting up the AP if it is present, determining whether the AP has

[2] The Office Action must provide specific, objective evidence of record for a finding of a suggestion or motivation to combine reference teachings and must explain the reasoning by which the evidence is deemed to support such a finding. *In re Sang Su Lee*, 277 F.3d 1338, 61 USPQ2d 1430 (Fed. Cir. 2002).

[3] The fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990); MPEP § 2143.01.

[4] *See* Natu at column 2, line 57 through column 3, line 12.

> passed its BIST, and selecting the AP to take the place of the designated BSP if the AP has passed its BIST. The BSP then designates the selected AP as the BSP instead of itself. The bootstrap indicator bit of the selected AP is set to indicate that the AP is the BSP. The bootstrap indicator bit of the designated BSP is cleared. (Emphasis added).

Thus, Natu concerns allowing a multiprocessor computer system to initialize properly, even when the processor that is designated as a the BSP after a hard reset of the computer system, fails. This contradicts the statement made in the Office Action that, "if the failing processor has internal failure, it may not be able to operate properly to remove itself from the operation" Therefore, the rational used in the Office Action for supporting the proposed combination of Natu and Kennedy is not supported by, and is contradicted by, the statements in the written description of Natu. Far from showing a motivation to combine their teachings, the cited patents "teach away" from the invention claimed.

Further, since Natu states, "The designated BSP then selects a processor from among the APs that will take the place of the designated BSP," the statements made in the Office Action with respect to "disabling the failed processor eliminates the problem of relying on a failed processor" would destroy the stated purpose[5] of Natu by disabling the device in Natu designated to select a processor to take the place of the designated BSP.

Because the statements in the Office Action used as a rational for forming the proposed combination of Natu and Kennedy are not supported by Natu or Kennedy, or by any other evidence of record, and because the statements made in the Office Action would result in destroying the stated purpose of Natu, the Office Action fails to meet the requirements for showing a teaching, suggestion, or motivation for making the proposed combination of Natu and Kennedy. By failing to meet these requirements, the Office Action cannot meet its burden for making a *prima facie* case of obviousness with respect to the rejection of claims 1-5.

Claims 1-5 are not obvious in view of the proposed combination of Natu and Kennedy because the proposed combination of Natu and Kennedy fails to disclose or suggest the claimed subject matter included in claims 1-5.

[5] If a proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984); MPEP § 2143.01.

Even if the requirements for combining the cited patents were met, claims 1-5 are not obvious in view of the proposed combination of Natu and Kennedy because the proposed combination of Natu and Kennedy fails to disclose or suggest the claimed subject matter included in claims 1-5. By way of example, but not limited to this example, independent claim 1 as now amended includes:

> designating one processor as a bootstrap processor;
> **providing a reset signal that starts a watchdog timer timing;**
> testing the bootstrap processor to verify that it will run BIOS code;
> **setting a latch for disabling said bootstrap processor** if the testing indicates a failure to run BIOS code or **if the watchdog timer times out;**
> **starting a control unit timer** for providing a time limit for a power on self-test;
> testing during [[a]] the power on self-test the operation of said bootstrap processor;
> testing during a built-in self-test the operation of said bootstrap processor;
> **setting a latch for disabling said bootstrap processor if the control unit timer times out;**
> assigning the bootstrap process to another processor if said bootstrap processor fails a test;
> said testing steps being implemented in an appliance server management system. (Emphasis added).

Thus, independent claim 1 includes, "providing a reset signal that starts a watchdog timer timing," and "setting a latch for disabling said bootstrap processor if the testing indicates a failure to run BIOS code or if the watchdog timer times out." Further, independent claim 1 also includes, "starting a control unit timer for providing a time limit for a power on self-test," and "setting a latch for disabling said bootstrap processor if the control unit timer times out."

The Office Action states,[6] "However, Natu fails to teach setting a latch for disabling the failed bootstrap processor if the testing indicates a failure." The Office Action relies on Kennedy as describing the subject matter quoted above as required in independent claim 1.

[6] *See* the Office Action on page 4, lines 12-13.

For reasons analogous to those stated above with respect to independent claims 6 and 12, Kennedy also fails to disclose or suggest the subject matter included in independent claim 1 as quoted above. Thus, the proposed combination of Natu and Kennedy fails to disclose or even to suggest the subject matter included in independent claim 1.

Because the proposed combination of Natu and Kennedy fails to disclose or suggest all of the subject matter included in independent claim 1, independent claim 1 is not obvious in view of the proposed combination of Natu and Kennedy.

Dependent claims 2-5 depend from independent claim 1, and so includes all of the subject matter included in independent claim 1, and more. For at least the reasons stated above with respect to independent claim 1, the proposed combination of Natu and Kennedy fails to disclose or suggest the subject matter included in dependent claims 2-5. Therefore, claims 2-5 are not obvious in view of the proposed combination of Natu and Kennedy.

For at least the reasons stated above with respect to the rejection of claims 1-5, Applicant respectfully requests reconsideration and withdrawal of the 35 U.S.C. § 103(a) rejection, and allowance of claims 1-5.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney ((612) 371-2132) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

SON H. LAM

By their Representatives,
SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
Attorneys for Intel Corporation
P.O. Box 2938
Minneapolis, Minnesota 55402
(612) 373-6904

Date DECEMBER 6/2006 By Robt B. Madden
Robert B. Madden
Reg. No. 57,521

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexendria, VA 22313-1450 on this 6th day of December 2006.

Amy Moriarty
Name

Signature